

A New Cascaded Switched-Capacitor Multilevel Inverter Based on Improved Series-Parallel Conversion with Less Number of Components

Elyas Zamiri, Naser Vosoughi, Seyed Hossein Hosseini, *Member, IEEE*, Reza Barzegarkhoo and Mehran Sabahi

Abstract— The aim of this study is to present a new structure for switched-capacitor multilevel inverters (SCMLIs) which can generate a great number of voltage levels with optimum number of components for both symmetric and asymmetric value of dc voltage sources. Proposed topology consists of a new switched-capacitor dc/dc converter (SCC) which has boost ability and can charge capacitors as self-balancing by using proposed binary asymmetrical algorithm and series-parallel conversion of power supply. Proposed SCC unit is used in new configuration as a sub-multilevel inverter (SMLI) and then, these proposed SMLIs are cascaded together and create a new cascaded multilevel inverter topology which is able to increase the number of output voltage levels remarkably without using any full H-bridge cell and also can pass the reverse current for inductive loads. In this case, two half bridges modules besides two additional switches are employed in each of SMLI units instead of using a full H-bridge cell which contribute to reduce the number of involved components in the current path, value of blocked voltage, the variety of isolated dc voltage sources and as a result the overall cost by less number of switches in comparison with other presented topologies. The validity of the proposed SCMLI has been carried out by several simulation and experimental results.

Index Terms— Cascade sub-multilevel inverter, series-parallel conversion, self-charge balancing, switched-capacitor

I. INTRODUCTION

MULTILEVEL inverters (MLIs) are known as one of the most popular solutions to improve the performance of renewable energy systems, electric vehicles (EVs) and other innovative power electronic utilities in medium and high power applications [1]-[2]. These converters can generate a

staircase voltage waveform at the output with high quality and desired spectrum. The desired output voltage is synthesized by appropriate switching of several dc voltage links which leads to decrease voltage stresses on switches and total harmonic distortion (THD) [3],[4].

In general, there are three conventional types of MLI configurations categorized into diode clamped (DCMLI) [5], flying capacitors (FCMLI) [6],[7] and cascade H-bridge topologies (CHB) which can be divided into two entire divisions based on symmetric and asymmetric value of dc power supplies [8]-[10].

Although these converters have a lot of advantages over the classic inverters, using aforementioned conventional topologies needs more number of required power switches, power supplies and large capacitor banks. Furthermore voltage of the capacitors tends to be discharged theoretically and therefore charge balancing control processing is necessary. There have been several suggested charge balancing circuits to control the capacitors' voltage [11]-[17].

[11]-[13] could regulate the duty cycle of dc bus capacitors for FCMLIs by using the existing redundancy switching states (RSSs). In this case, the accuracy of proposed approach depends on designing a close loop control system. Also, [14] presented a phase-shift modulation approach to obviate the discharging problem in a capacitor-based 7-level CHB topology supplied by one dc voltage source for main unit and one floating capacitor for auxiliary unit. Here, the main and auxiliary power switches have to drive by fundamental and high switching frequency, respectively. Meanwhile, [15] presented a triplen harmonic compensatory method based on fundamental switching strategy to extend the range of modulation index for three phase utility of 7-level CHB topology. Using the resonant switched capacitor circuit (RSCC) as an external voltage balancing network can also prevent this problem for DCMLIs [16].

Nowadays, many researchers have presented numerous developed structures of MLIs with less number of key components such as number of required switches, gate drivers, power supplies and so on [18]-[20]. One of the most particular schemes of them is switched-capacitors multilevel inverters (SCMLIs). These converters can produce more output voltage levels with less number of required power supplies [21]-[24]. SCMLIs contain several capacitors and switches which can connect dc power supply to ac output and are able to decrease the burden of power supply to achieve higher number of

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Elyas Zamiri, Naser Vosoughi, Seyed Hossein Hosseini and Mehran Sabahi are with the faculty of Electrical and Computer Engineering of University of Tabriz, Tabriz, Iran. (Authors' E-mail: elyaszamiri@yahoo.com, naser.vosoughi@yahoo.com, hosseini116j@yahoo.com).

Reza Barzegarkhoo is with faculty of Electrical Engineering Sahand University of Technology (SUT), Tabriz, Iran (Email: barzegar_sina@yahoo.com.au).

voltage levels.

Nevertheless, to attain the greater number of output voltage levels with less number of power semiconductors and simple commutation, a new type of SCMLIs have been emerged using the series/parallel switching strategy (SCISPC)[25],[26]. The distinctive features of these types of inverters are that they can increase the flexibility of systems by switching between several capacitors in series or parallel modes and therefore can transfer more input power to the output. In this way, [27] and [28] presented a new family of cascade and hybrid SCISPC topologies which have a modular structure and generate more output voltage levels with least of switches. But such structures have used the full H-bridge units with isolated dc voltage sources to change the polarity of output voltage waveform which makes more conducting loss through the current path components and increases the number of power switches.

In this paper, initially a new switched-capacitor dc/dc converter (SCC) is presented which can switch as conventional series/parallel conversion and generate multiple dc link voltages with optimum components. In this case, voltage of all capacitors is filled by binary asymmetrical pattern without using any auxiliary circuits. At the next, a new sub-multilevel inverter topology presents which is performed based on proposed SCC unit and without using full H-bridge cell. In addition, this structure is suitable for an inductive load with capability to pass the reverse current. After that, proposed sub-multilevel modules are cascaded with each other and create more output voltage levels. Therefore most of the parameters such as number of required switches, diodes, maximum current path components and value of total blocked or standing voltage are improved. In order to prove the performance of the proposed circuit, variety number of comparisons with other recently suggested topologies has been done in fair conditions and also analysis of theoretical power losses is given. Finally validity of the proposed topology is shown by several experimental and simulation results.

II. PROPOSED SCC

Fig. 1(a) shows basic circuit of the proposed SCC. This circuit is named by basic unit and contains one dc power supply, one capacitor, one passive power diode and two active power switches. Photovoltaic (PV) cells, batteries and fuel cells can be used as a power supply in this structure. Fig. 1 (b) and (c) show that how to carry out the charging and discharging operations for capacitor C. Switches S_a and S_b are used in series and parallel conversion, respectively. As it can be inspected, when the switch S_b becomes ON, the capacitor C is charged to V_{dc} and when the switch S_a turns ON, the diode becomes reverse biased and capacitor is discharged. In this mode, the power supply energy and stored energy of C are transferred to the output. It is obvious that, basic unit does not need any extra charge balancing control circuits and complicated commutation methods which is

counted as a great merit of this structure [28]. Also, it is remarkable that, the internal resistance of power diode and capacitor can damp the unequal voltage between capacitor and dc voltage source during the charging operation which leads to introduce an effective and practical power circuit.

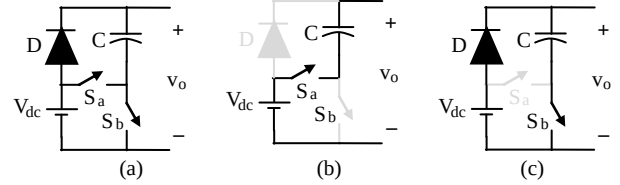


Fig. 1 (a) Basic series/parallel unit (b) Capacitor discharging mode (c) Capacitor charging mode

In the next step, proposed dc/dc converter is made by extended connection of this basic unit. Then a staircase voltage waveform is generated at the output with capability of passing the reverse current for inductive load and can be used as a part of inverters. Fig. 2 shows circuit configuration of the proposed converter. In order to charge all of the capacitors and generate output voltage waveform, the switches S_{ai} ($i=1,2,...,n-1$), S_{bi} and S_{ci} ($i=1,2,...,n$) are driven by series/parallel conversion or combination of them.

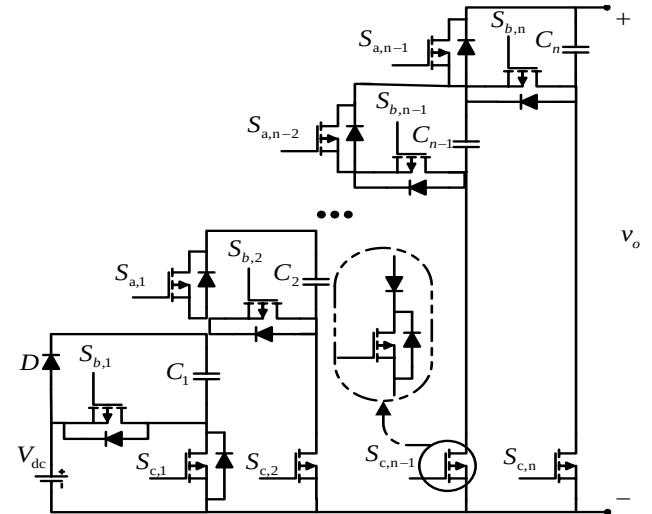


Fig. 2 Proposed switched capacitor dc/dc converter (SCC)

In this case, switches S_{ci} are unidirectional power switches without antiparallel diode which can pass the reverse inductive load current and other switches are also unidirectional with internal antiparallel diode. As figure shows, switches S_{ci} ($i=2,3,...,n$) can be substituted by ordinary power switches and a series diode to counteract the effect of internal antiparallel diode. Table I indicates the different switching and capacitors' states for proposed SCC.

In this table, 0 and 1 mean OFF and ON switching state and C and D refer to charging and discharging modes for capacitors, respectively. In order to generate more number of output voltage levels with optimum number of components, all of the capacitors should be charged by binary asymmetrical algorithm, according to this table in such a way that, in state (1) when switch $S_{c,1}$ becomes ON, capacitor C_1 is charged to

V_{dc} and this voltage level is transferred to the output through $S_{a,i}$ ($i = 1, 2, \dots, n-1$) simultaneously.

Also in state (2), C_2 is being charged to $V_{dc} + V_{c1}$ through switch $S_{c,2}$ and with discharging of C_1 , second voltage level generates at the output through $S_{a,i}$ and $S_{b,1}$, simultaneously which is equal to $2V_{dc}$. After this moment, without entering other capacitors into the circuit, voltage level of $3V_{dc}$ can be transferred to the output by stored voltage of C_2 and constant dc voltage source. In this moment, C_1 is again charged by dc voltage source directly and for next voltage level, this stored voltage besides the across voltage of C_2 and constant dc voltage source are transferred to the output which is equalized to $4V_{dc}$ and this consecutive operation continues so on.

TABLE I
SWITCHING AND CAPACITORS STATES OF PROPOSED SCC

v_o		V_{dc}	$2V_{dc}$	$3V_{dc}$	$4V_{dc}$	$\cdots$	$2^n V_{dc}$
Switching States	$S_{a,1}$	1	1	0	0	$\cdots$	0
	$S_{a,2}$	1	1	1	1	$\cdots$	0
	$\vdots$	1	1	1	1	$\cdots$	0
	$S_{a,n-1}$	1	1	1	1	$\cdots$	0
	$S_{b,1}$	0	1	0	1	$\cdots$	1
	$S_{b,2}$	0	0	1	1	$\cdots$	1
	$\vdots$	0	0	0	0	$\cdots$	1
	$S_{b,n}$	0	0	0	0	$\cdots$	1
	$S_{c,1}$	1	0	1	0	$\cdots$	0
	$S_{c,2}$	0	1	0	0	$\cdots$	0
	$\vdots$	0	0	0	$\vdots$	$\cdots$	0
	$S_{c,n}$	0	0	0	0	$\cdots$	0
Capacitors States	C_1	C	D	C	D	$\cdots$	D
	C_2	-	C	D	D	$\cdots$	D
	C_3	-	-	-	C	$\cdots$	D
	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\cdots$	$\cdots$	D
	C_n	-	-	-	-	C	D

The prominent feature of proposed circuit is that by entering the next capacitors into the circuit and also continuing the series-parallel switching strategy, the number of output voltage levels is enhanced as binary manner from V_{dc} to $2^n V_{dc}$.

It is important to note that, always at each of voltage steps, the pertinent capacitor of previous steps must be connected as parallel to keep on the charging operation. Therefore, if we assume the number of capacitors equal to n , the stored voltage of each capacitor would be equalized to:

$$V_{C,k} = 2^{k-1} V_{dc} \quad \text{for } k = 1, 2, \dots, n \quad (1)$$

Also from this table it is obvious that, proposed SCC is able to generate different positive output voltage levels by self-balancing ability. Now by considering the proposed overall structure (Fig. 2), number of required switches ($N_{switch,u}$) or gate drivers ($N_{Driver,u}$), number of required isolated-gate bipolar transistors (IGBTs) ($N_{IGBT,u}$), power diodes

($N_{diode,u}$) and output voltage levels ($N_{level,u}$) are calculated by the following equations, respectively:

$$N_{switch,u} = N_{Driver,u} = N_{IGBT,u} = 3n - 1 \quad (2)$$

$$N_{diode,u} = n \quad (3)$$

$$N_{level,u} = 2^n \quad (4)$$

According to (4), proposed circuit has appropriate performance as boost capability. This factor can be defined as:

$$\beta = \frac{V_{o,max,u}}{\sum V_{dc}} = 2^n \quad (5)$$

Moreover, this structure is able to mitigate the total blocked voltage. As well-known, the value of blocked voltage should be tolerated by switches and means standing voltage across of switches which effects on conduction losses, efficiency and cost [29]. In this case, total blocked voltage is formulized by:

$$V_{block,u} = [3(2^n - 1) - 1] V_{dc} \quad (6)$$

III. PROPOSED SUB-MULTILEVEL INVERTER

As it was analysed before, proposed SCC generates output voltage waveform with positive polarity. Therefore it is not suitable for inverter applications. In order to change the polarity and create an AC waveform, an H-bridge cell can be connected to the output similar to other existing structures. However this cell may increase the number of required IGBTs and number of involved components in the current path. This paper has not focused on added H-bridge cell and presents a new scheme of SCISP shown in Fig. 3, based on two utilized half-bridges.

In order to convert the output polarity of SCC and create all of the voltage levels (even and odd) at the output, this structure always requires pair stage of SCC units. Therefore, proposed SCISP named as sub-multilevel inverter (SMLI) can produce positive, zero and negative output voltage levels with six unidirectional power switches and two same units of SCC. As a result, $2n$ capacitors and two isolated dc power supplies are needed for this structure.

Now, number of required IGBTs or gate drivers and number of power diodes can be expressed as (7) and (8) respectively.

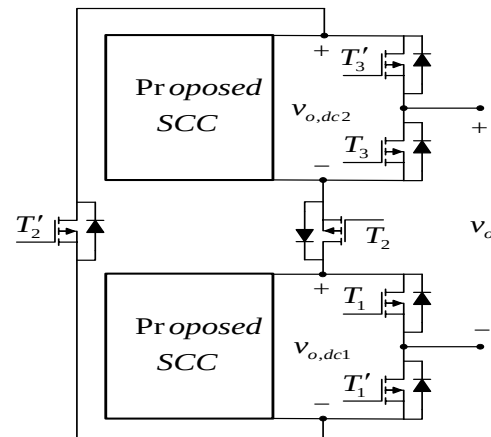


Fig. 3 Proposed SMLI configuration

$$N_{IGBT_{Sub}} = N_{Driver_{Sub}} = 6n + 4 \quad (7)$$

$$N_{Diode_{Sub}} = 2n \quad (8)$$

Table II indicates ON switching states of proposed SMLI which is summarized by seven different modes. According to this table, to refrain from short circuit problems, switches of (T_1, T'_1) , (T_2, T'_2) and (T_3, T'_3) , are triggered as complementary operation with each others and should not to be ON simultaneously. Also this structure can work on symmetric and asymmetric value of dc voltage sources. In symmetric structure, all of the dc sources are equal and that are different in asymmetric topology. Then, with considering (1), to obtain maximum number of voltage levels from asymmetric condition, the value of other isolated dc power supply should conform the following experssion:

$$V_{dc,2} = (1 + 2^n) V_{dc,1} \quad (9)$$

Table III indicates the pertinent equations of $N_{level_{Sub}}$, $V_{o,max_{Sub}}$ and $V_{Blocked_{Sub}}$ for symmetric and asymmetric forms in proposed SMLI. In this case, the asymmetric calculations in table III are done by considering (9).

TABLE II
SWITCHING PATTERN OF PROPOSED SUB-MULTILEVEL INVERTER

	ON Switches	V_o
Switching States	1 T'_1, T'_2, T'_3	$V_{o,dc1} + V_{o,dc2}$
	2 T_1, T_2, T'_3	$V_{o,dc2}$
	3 T'_1, T_2, T_3	$V_{o,dc1}$
	4 T_1, T_2, T_3	0
	T'_1, T'_2, T'_3	
	5 T_1, T'_2, T'_3	$-V_{o,dc1}$
	6 T'_1, T'_2, T_3	$-V_{o,dc2}$
	7 T_1, T_2, T_3	$-V_{o,dc1} - V_{o,dc2}$

To achieve the greater number of voltage levels, proposed SMLI can be extended by increasing the number of output voltage levels for proposed SCC. But this way yields to some identical restrictions due to increase the voltage drop and existed spikes across each of capacitors especially in high power ratio. To avoid this consternain, the best solution to increase the number of voltage levels is considered by series connection of proposed SMLIs with each other shown as proposed cascaded sub-multilevel inverter (CSMLI) in Fig. 4. In this figure, number of casceded SMLI units is indexed by m . As a result, output voltage of proposed CSMLI is obtained by:

$$V_o(t) = V_{o,1}(t) + V_{o,2}(t) + \dots + V_{o,m}(t) \quad (10)$$

It should be noted that, in this case, the number of capacitors which have been used in each of SCCs is assumed same. To reduce the cost, weight, total blocked voltage and some other identical problems, the required capacitors for each of proposed SCC units (n) is optimized in next section.

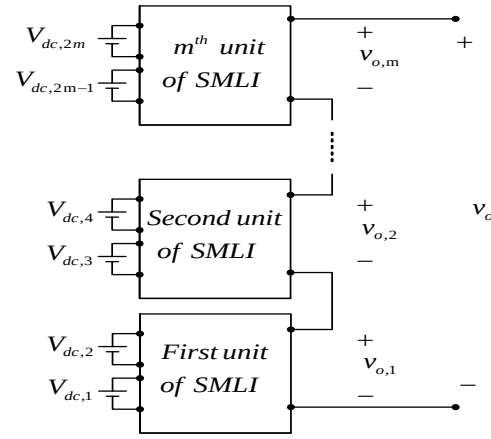


Fig. 4 Proposed cascaded sub-multilevel inverter (CSMLI)

TABLE III
DIFFERENT RELATED EQUATIONS FOR PROPOSED SMLI TOPOLOGY

Parameters	Symmetric	Asymmetric
$N_{level_{Sub}}$	$1 + 2^{n+2}$ (11)	$1 + 2^{n+2} + 2^{2n+1}$ (14)
$V_{o,max_{Sub}}$	$2^{n+1} V_{dc}$ (12)	$[2^{n+1} + 2^{2n}] V_{dc}$ (15)
$V_{block_{Sub}}$	$2 \sum_{j=1}^3 V_{block,Tj} + \sum_{j=1}^2 V_{block,uj}$ (13) $= [(7 \times 2^{n+1}) - 8] V_{dc}$	$2 \sum_{j=1}^3 V_{block,Tj} + \sum_{j=1}^2 V_{block,uj}$ (16) $= [2^{2n+2} + 2^{n+3}] V_{dc}$

IV. PROPOSED IMPROVED CSMLI

In this section, the number of requierd capacitors in each of proposed SMLI units is optimized from the view point of maximum produced output voltage levels for proposed CSMLI with minimum number of IGBTs. This optimization is done based on asymmetric value of dc sources according to (9). In general, the number of output voltage levels for proposed CSMLI is obtained by:

$$N_{level} = \left(N_{level_{Sub}} \right)^m \quad (17)$$

Where $N_{level_{Sub}}$ is the number of output voltage levels for proposed SMLI which is calculated by (14). Then equation of (17) can be rewritten as:

$$N_{level} = \left(2^{n+2} + 2^{2n+1} + 1 \right)^m \quad (18)$$

On the other hand, the relation of m in terms of N_{IGBT} (number of required IGBTs for proposed CSMLI) and $N_{IGBT_{Sub}}$ is equalized to (19):

$$m = \frac{N_{IGBT}}{N_{IGBT_{Sub}}} \quad (19)$$

Also with inserting (13) into (18) and (19):

$$N_{level} = \left(2^{n+2} + 2^{2n+1} + 1 \right)^{\frac{N_{IGBT}}{6n+4}} \quad (20)$$

In order to obtain the optimal number of capacitor from each of SMLIs, the variation of N_{level} against N_{IGBT} for specific number of n , is curved according to (20) and illustrated by

Fig. 5. As figure shows, for constant value of N_{IGBT} , N_{level} has been maximized when one capacitor is being used. Therefore with respect to $n=1$, number of output voltage levels, required IGBTs, power diodes and total value of blocked voltage for proposed improved CSMLI are obtained for both symmetric and asymmetric conditions and are summarized by Table IV. In addition, based on (9), the value of dc voltage sources in i^{th} unit of proposed CSMLI should be adopted by:

$$V_{dc2,i} = 3V_{dc1,i} = 3(17^{i-1})V_{dc} \quad i = 1, 2, \dots, m \quad (21)$$

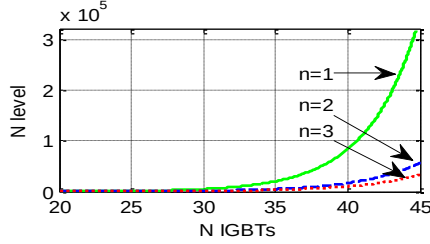


Fig. 5. Variation of N_{level} against N_{IGBT} for different values of n

Fig.6. shows an improved CSMLI configuration with considering $m=1$ which lead to generate 17-level output voltage based on proposed asymmetric topology. In this circuit, the values of dc isolated power supplies are set on V_{dc} and $3V_{dc}$ according to (9). Table V shows the switching pattern of proposed 17-level inverter.

TABLE IV
DIFFERENT RELATED CALCULATIONS OF PROPOSED IMPROVED CSMLI

Parameters	Symmetric	Asymmetric
N_{level}	$8m+1$ (22)	17^m (25)
$v_{o,max}$	$4mV_{dc}$ (23)	$\frac{17^m - 1}{2}$ (26)
V_{block}	$m \times [2 \sum_{j=1}^3 V_{block,Tj} + \sum_{j=1}^2 V_{block,ij}]$ $= 20mV_{dc}$ (24)	$\sum_{k=1}^m (2 \sum_{j=1}^3 V_{block,Tj,k} + \sum_{j=1}^2 V_{block,ij,k})$ $= \frac{5(17^m - 1)}{2}$ (27)
N_{IGBT}	$10m$ (28)	
N_{Diode}	$2m$ (29)	

In this case, all of the switches are driven by fundamental switching frequency whereas the sinusoidal reference voltage is compared with some available dc voltage levels and create the related gate switching pulses. The most advantage of this switching method is referred to low switching frequency which yields to reduction of switching loss [29],[30]. Details of fundamental switching modulation strategy are not objective of this paper. In addition from table V, it is clear that, to generate each of output voltage levels, only five switches are being involved in the current path.

At this stage, to determine the capacitance of C_1 and C_2 , two assumptions are considered which one is related to output sinusoidal load current with phase difference between output voltage and current (ϕ) and the other is contribute to same duration in each step of staircase output voltage. Thus, the

maximum discharging amount of each capacitor can be defined as (30) in one half cycles:

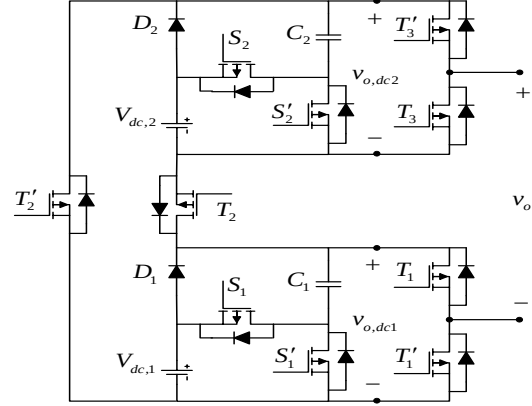


Fig. 6. Proposed 17-level structure

TABLE V
DIFFERENT SWITCHING AND CAPACITORS STATES OF PROPOSED 17-LEVEL INVERTER

	ON Switches	v_o	C_1	C_2
Switching States	1 $T'_1, T_2, T'_3, S'_1, S_2$	$4V_{dc} + v_{c,1} + v_{c,2}$	D	D
	2 $T'_1, T_2, T'_3, S'_1, S_2$	$4V_{dc} + v_{c,2}$	C	D
	3 $T_1, T_2, T'_3, S'_1, S_2$	$3V_{dc} + v_{c,2}$	C	D
	4 $T'_1, T_2, T'_3, S'_1, S'_2$	$4V_{dc} + v_{c,1}$	D	C
	5 $T'_1, T_2, T'_3, S'_1, S'_2$	$4V_{dc}$	C	C
	6 $T_1, T_2, T'_3, S'_1, S'_2$	$3V_{dc}$	C	C
	7 $T'_1, T_2, T_3, S'_1, S'_2$	$V_{dc} + v_{c,1}$	D	C
	8 $T'_1, T_2, T_3, S'_1, S'_2$	V_{dc}	C	C
	9 $T_1, T_2, T_3, S'_1, S'_2$	0	C	C
	$T'_1, T'_2, T'_3, S'_1, S'_2$			
	10 $T_1, T'_2, T'_3, S'_1, S'_2$	$-V_{dc}$	C	C
	11 $T_1, T'_2, T'_3, S'_1, S'_2$	$-V_{dc} - v_{c,1}$	D	C
	12 $T'_1, T'_2, T'_3, S'_1, S'_2$	$-3V_{dc}$	C	C
	13 $T_1, T'_2, T'_3, S'_1, S'_2$	$-4V_{dc}$	C	C
	14 $T_1, T'_2, T'_3, S'_1, S'_2$	$-4V_{dc} - v_{c,1}$	D	C
	15 $T'_1, T'_2, T'_3, S'_1, S'_2$	$-3V_{dc} - v_{c,2}$	C	D
	16 $T_1, T'_2, T'_3, S'_1, S'_2$	$-4V_{dc} - v_{c,2}$	C	D
	17 $T_1, T'_2, T'_3, S'_1, S'_2$	$-4V_{dc} - v_{c,1} - v_{c,2}$	D	D

$$Q_{Ci} = \int_{t_i}^{T/4 - t_j} I_{out} \sin(2\pi f_s t - \phi) dt \quad i = 1, 2 \quad (30)$$

Where T , f_s and I_{out} are period of one cycle, frequency of output voltage and amplitude of load current, respectively and also $[t_j, T/4 - t_j]$ is time interval corresponded to the longest discharging cycle (LDC) of each capacitors. On the other hand, in proposed 17-level inverter, this time interval varies for C_1 and C_2 . According to Table V, the LDC for C_1 and C_2 are illustrated by Fig.7. Thus, with considering the kV_{in} as maximum allowable voltage ripple, the optimum value of capacitors can be taken by:

$$C_{opt,i} \geq \frac{Q_{Ci}}{kV_{in}} \quad (i=1,2) \quad (31)$$

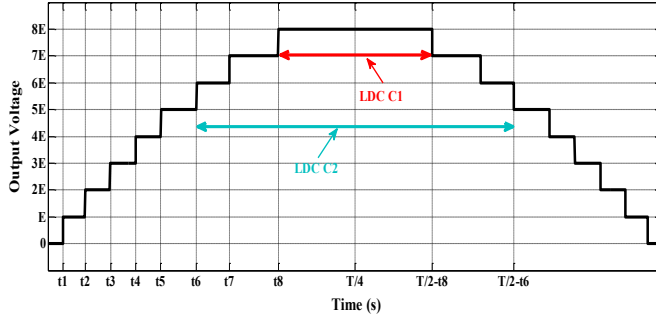


Fig. 7 Typical output voltage waveform of 17-level inverter for positive half cycle

V. POWER LOSS ANALYSIS

In this section, theoretical total power losses and overall efficiency of proposed improved CSMLI based on ($m=1$) are calculated. For this kind of converters, always three major types of associated losses should be considered which include: switching losses (P_{sw}), conduction losses of semiconductor devices (P_{con}) and ripple losses of two utilized capacitors (P_{rip}). All of calculations are done based on fundamental switching frequency strategy [29].

A. Switching losses

Switching loss occurs during the ON and OFF period of switching states. For simplicity, a linear approximation between voltage and current of switches in the switching period is considered. Based on this assumption, the following equations can be expressed for i^{th} involved power switch:

$$P_{sw,on,i} = f_{sw} \int_0^{t_{on}} v_{on,i}(t) i(t) dt = f_{sw} \int_0^{t_{on}} \left(\frac{V_{on,i}}{t_{on}} t \right) \left(-\frac{I_i}{t_{on}} (t - t_{on}) \right) dt \quad (32)$$

$$= \frac{1}{6} f_{sw} V_{on,i} I_i t_{on}$$

$$P_{sw,off,i} = f_{sw} \int_0^{t_{off}} v_{block,i}(t) i(t) dt = f_{sw} \int_0^{t_{off}} \left(\frac{V_{block,i}}{t_{off}} t \right) \left(-\frac{I'_i}{t_{off}} (t - t_{off}) \right) dt \quad (33)$$

$$= \frac{1}{6} f_{sw} V_{block,i} I'_i t_{off}$$

Where I_i and I'_i are the currents which pass through i^{th} power switch after turning ON and before turning OFF, respectively and f_{sw} is the switching frequency equalized to the reference frequency. In order to calculate the total switching loss, the number of ON (N_{on}) and the number of OFF (N_{off}) switching states per one cycle should be multiplied by (32) and (33) according to (34):

$$P_{sw} = \sum_{i=1}^{10} \left(\sum_{k=1}^{N_{on}} P_{sw,on,ik} + \sum_{k=1}^{N_{off}} P_{sw,off,ik} \right) \quad (34)$$

B. Conduction losses

To calculate the total conduction losses of each component, a straightforward method based on pure-resistance load is

presented. Regarding Table V, three possible operating modes can be investigated including discharging states for both capacitors (states number of 1 and 17), charging states for both capacitors (states number of 5,6,8,10,12 and 13) and discharging states for one capacitor and charging states for another one or vice versa (other remaining states).

Fig. 8 (a)-(c) demonstrate the equivalent circuits of charging and discharging operating modes for capacitors. In these figures, R_{on} , R_D , r_{ESR} , R_L and V_F are internal ON-state resistance of each switch, internal resistance of each diode, equivalent series resistance (ESR) of each capacitor, load resistance and the forward voltage drop of each incurred diode, respectively.

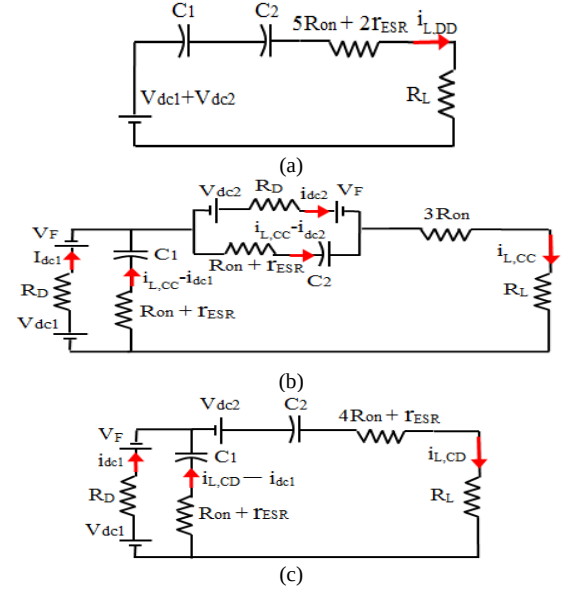


Fig. 8. The equivalent circuit of proposed 17-level structure with a resistive load (a) in discharging modes (b) in charging modes (c) in combination of charging and discharging modes

According to Fig. 8 (a) during the series connection of capacitors to the respective dc voltage sources, the value of load current can be written as:

$$i_{L,DD} = \frac{4V_{dc} + v_{c,1} + v_{c,2}}{5R_{on} + 2r_{ESR} + R_L} \quad (35)$$

Therefore, the instantaneous conduction loss ($p_{c,DD}$) and average conduction loss ($\overline{p_{c,DD}}$) for one full cycle of discharging mode with respect to time intervals of Fig. 7 and Table V, can be calculated as following, respectively:

$$p_{c,DD} = (5R_{on} + 2r_{ESR}) i_{L,DD}^2 \quad (36)$$

$$\overline{p_{c,DD}} = \frac{2f_{sw}}{\pi} \left(\frac{\pi}{2} - t_b \right) p_{c,DD} \quad (37)$$

Also, with respect to Fig. 8 (b) and with considering the time intervals between states of 3 and 5 and also states of 1 and 2 in Fig. 7, the instantaneous and average value of conduction losses for charging modes of both capacitors ($p_{c,CC}$ & $\overline{p_{c,CC}}$), are driven by (38) and (39) respectively:

$$p_{c,CC} = 3R_{on} i_{L,CC}^2 + R_D (i_{dc,1}^2 + i_{dc,2}^2) + (R_{on} + r_{ESR}) [(i_{L,CC} - i_{dc,1})^2 + (i_{L,CC} - i_{dc,2})^2] \quad (38)$$

$$\overline{p_{c,CC}} = \frac{2f_{sw}}{\pi} [(t_5 - t_3) + (t_2 - t_1)] p_{c,CC} \quad (39)$$

Where, $i_{dc,1}$ and $i_{dc,2}$ can be calculated by using the Kirchhoff voltage law (KVL) according to following, respectively:

$$i_{dc,1} = \frac{(r_{ESR} + R_{on})i_{L,CC} + V_{dc} - v_{c,1} - V_F}{R_D + r_{ESR} + R_{on}} \quad (40)$$

$$i_{dc,2} = \frac{(r_{ESR} + R_{on})i_{L,CC} + 3V_{dc} - v_{c,2} - V_F}{R_D + r_{ESR} + R_{on}} \quad (41)$$

In addition, by considering the Fig. 8 (c) and Fig. 7, when capacitor of $C_1(C_2)$ is charged (discharged) and $C_2(C_1)$ is discharged (charged), the instantaneous and average conduction losses can be expressed as (42) and (43), respectively:

$$P_{c,CD,i} = (4R_{on} + r_{ESR})i_{c,CD}^2 + R_D i_{dc,i}^2 + (R_{on} + r_{ESR})(i_{c,CD} - i_{dc,i})^2 \quad \text{for } i = 1, 2 \quad (42)$$

$$\overline{p_{c,CD}} = \frac{2f_{sw}}{\pi} [(t_8 - t_6)] p_{c,CD,2} + [(t_6 - t_5) + (t_3 - t_2)] p_{c,CD,1} \quad (43)$$

As a result, total value of conduction losses (P_{Con}) in one full cycle can be summarized by (44):

$$P_{Con} = \overline{p_{c,DD}} + \overline{p_{c,CC}} + \overline{p_{c,CD}} \quad (44)$$

Fig. 9 shows the variation of load current stresses versus load resistance. As it can be found, the maximum value of short circuit current ($i_{sc,max}$) is being occurred in the charging mode operation ($i_{L,CC}$) and therefore this value must be tolerated by incurred components among the three defined modes.

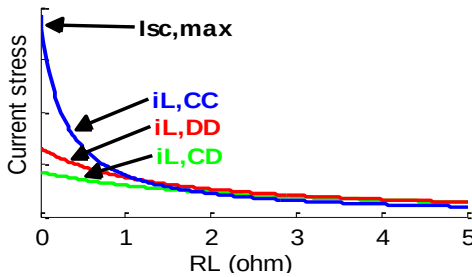


Fig. 9. Variation of current stresses versus R_L in three defined modes

C. Ripple losses

When the capacitors are connected in parallel for charging operation, the ripple losses occur by the difference between the respective input voltage and the across voltage of capacitors ($v_{c,i}$ ($i = 1, 2$)) [25]. Therefore, the ripple voltage of capacitors (ΔV_{Ci}) is taken from:

$$\Delta V_{Ci} = \frac{1}{C_i} \int_{t'}^t i_{Ci}(t) dt \quad (45)$$

Where, $i_{Ci}(t)$ is the passing current of capacitor and $[t' - t]$ is that time interval for charging modes which can be attained by regarding Table V. Thus, the total value of ripple loss, for one full cycle of output waveform is equalized to (46).

$$P_{Rip} = \frac{f_{sw}}{2} \sum_{i=1}^2 C_i \Delta V_{Ci}^2 \quad (46)$$

From (45) and (46), it is clear that, P_{Rip} is inversely proportional to the capacitance C_i which means larger capacitance contributes to higher value of overall efficiency. Moreover, based on above analysis, in order to design the proposed converter, two main identical restrictions must be considered which are expressed as following:

$$I_{out,max} \leq \frac{i_{sc,max}}{\lambda} \quad (47)$$

$$V_{out,max} \leq \frac{V_{Block}}{\lambda} \quad (48)$$

Where, λ , $V_{out,max}$ and $I_{out,max}$ are a safety coefficient, maximum value of output voltage and current, respectively. Therefore, with respect to (47) and (48), the maximum value of output power ($P_{out,max}$) can be expressed as:

$$P_{out,max} \leq \frac{V_{Block} i_{sc,max}}{\lambda^2} \quad (49)$$

Finally, the overall efficiency of proposed improved CSMLI, can be defined by (50).

$$\eta = \frac{P_{out}}{P_{out} + P_{sw} + P_{Con} + P_{Rip}} \quad (50)$$

VI. COMPARISON DISCUSSION

In this section, proposed improved CSMLI is compared with several existing reduced components SCMLIs which have been recently presented. In this case, to have a fair survey, some of MLI topologies which are capable of being cascaded and also implemented by switched-capacitor technique, have been chosen. Comparisons are performed in both symmetric and asymmetric forms for proposed improved CSMLI, in different aspects at the same condition.

A. Symmetric inverters' comparison

Table VI proves the advantages of proposed symmetric improved CSMLI in contrast to symmetric conventional CHB, presented topology of [27] and two suggested structures of [28] in different mentioned aspects for a specific number of m and $N_{level} = 9$. Meanwhile, second presented structure of [28] cannot pass the reverse current. Then to have same condition in comparisons, a modified topology based on second presented structure of [28] is considered which some of its respected diodes have been replaced by power switches.

TABLE VI

SYMMETRIC COMPARISON FOR $N_{level} = 9$

Parameters	CHB	[27] & first top [28]	Mod second top [28]	Proposed improved CSMLI
N_{IGBT}	16	12	12	10
N_{diode}	0	2	2	2
$N_{capacitor} = N_{dc}$	4	2	2	2
V_{block}	$16V_{dc}$	$20V_{dc}$	$24V_{dc}$	$20V_{dc}$
$N_{Current, path, max}$	8	6	6	5

B. Asymmetric inverters' comparison

Fig. 10 (a) to (e) show the variations of maximum number of involved components in the current path, number of required IGBTs or gate drivers, power diodes, capacitors or variety of dc sources and value of blocked voltage versus number of output voltage levels in asymmetric comparison, respectively between proposed improved CSMLI and that suggested topologies presented in [27] and [28]. As it can be observed, due to non-using the output full H-bridge cells, proposed structure needs less number of components for

generating the same voltage levels at the output in contrast to others. Also, from the Fig.10 (e), the variation of blocked voltage for proposed CSMLI is accorded to presented topology of [27] and first structure of [28] in spite of the fact that they are being used a full H-bridge cell in their circuits, while proposed topology has used two half-bridge instead. Moreover, one of the most important remaining factors in comparison which may create a limitation for practical applications of asymmetric MLIs is addressed by dispersed value of isolated dc power supplies.

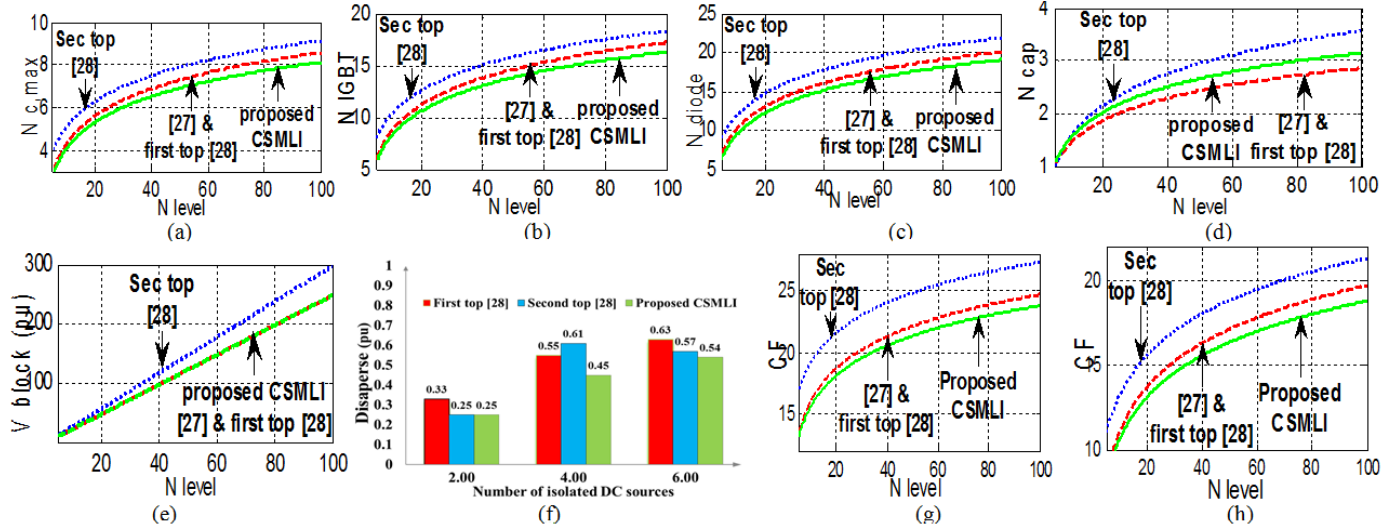


Fig. 10. Variations of (a) maximum number of current path components versus N_{level} (b) required IGBTs versus N_{level} (c) required diodes versus N_{level} (d) required capacitors versus N_{level} (e) value of blocked voltage versus N_{level} (f) dispersed value of dc power supply versus $N_{dc} = 2, 4, 6$ (g) CF versus N_{level} for $\alpha = 1.5$ (h) CF versus N_{level} for $\alpha = 0.5$

Because, in some especial utilities such as PV applications, providing the different value of dc power supplies is very difficult and can impose on overall costs. The per unit value of this factor can be defined as (51) and its respective variation is illustrated in Fig. 10 (f) for two, four and six number of isolated dc sources.

$$\sigma_{Disp}^{pu} = \frac{\sum_{i=1}^m \left| (V_{dc,i} - \frac{V_{o,max}}{m}) \right|}{V_{o,max}} \quad (51)$$

In addition, the value of σ_{Disp}^{pu} for proposed improved CSMLI structure is equalized to:

$$\sigma_{Disp}^{pu} = \frac{\sum_{i=1,3,\dots}^{2m-1} \left| (17)^{i-1} - \frac{17^m - 1}{4m} \right| + \sum_{i=2,4,\dots}^{2m} \left| 3(17)^{\frac{i}{2}-1} - \frac{17^m - 1}{4m} \right|}{\frac{17^m - 1}{2}} \quad (52)$$

From Fig. 10 (f), it can be discerned that, proposed structure has lower value of σ_{Disp}^{pu} in contrast to others.

The last parameter in comparison is related to estimation of overall cost. This factor can be expressed as (53) according to defined cost function (CF) of [18]. In this equation α is weight coefficient of blocked voltage versus number of IGBTs.

$$CF = N_{IGBT} + \alpha V_{Block}^{pu} = N_{IGBT} + \alpha \frac{V_{Block}}{V_{o,max}} \quad (53)$$

It is clear that the value of α varies. In general, if α selects greater than one, the value of blocked voltage will be important and on the other hand, if α chooses less than one, the number of IGBTs and their respected costs will be important to select the appropriate switching devices. Fig 10 (f) and (g) show the better overall cost condition of proposed improved CSMLI in contrast to others for $\alpha = 1.5$ and $\alpha = 0.5$, respectively.

VII. SIMULATION AND EXPERIMENTAL RESULTS

To prove the effectiveness of proposed topology, several simulation and experimental results for proposed 17-level inverter structure shown in Fig. 6 and a 49-level derived structure are presented in this section. For simulation, PSCAD/EMTDC software has been used and all of the semiconductor devices are assumed ideal. In addition, to generate gate switching pulses at fundamental switching frequency with respect to table V, the 89C52 microcontroller by ATMEL Company has been utilized in experimental tests. Also, the kind of utilized power MOSFETs and diodes are SPW47N60C3 (with antiparallel diode and $R_{on} = 70m\Omega$) and MUR1560G (with $R_D = 50m\Omega$), respectively which are capable of working on high voltage applications. The capacitance of two incurred capacitors in proposed circuit is assumed same and equal to $1800 \mu F$ with $r_{ESR} = 0.1\Omega$. To evaluate the overall

performance of proposed topology, three case studies are considered as follows:

A. First case study

In first case study, 400 W input power is applied to the load considered a series R-L load with values of $R = 150\Omega$ and $L = 320mH$. Meanwhile, the values of two isolated dc power supplies are set on 50 and 150 volts which would lead to generate 50 Hz 17-level output voltage. Fig. 11(a) and (b) show the steady state load voltage and current waveforms in simulation and experiment, respectively. As it can be seen, the maximum amplitude of load voltage and current are about 400 V and 2 A, respectively. The initial behavior of load voltage and current waveforms in transient state, based on simulation result is illustrated by Fig. 12. Fig. 13 (a) and (b) indicate the harmonic orders of load voltage and current based on simulation, respectively. Here, the defective lower harmonic orders are multiplied by ten. Also, Fig. 14 shows the no load condition of output voltage in experiment.

As it can be inspected, extracted results have good agreements with each other. Moreover, Fig. 15 (a) and (b) illustrate the balanced voltage waveform of two utilized capacitors in simulation and experiment, respectively.

As it can be seen, the across ripple voltage of capacitors has acceptable value and can mitigate the total ripple loss. Also, Fig. 16 shows experimental extracted results for blocked voltage of across switches S_1, S_2, T_1, T_2 and T_3 , respectively.

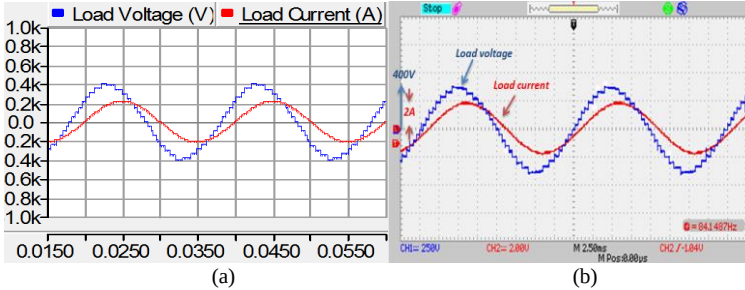


Fig. 11. Steady states output voltage and current waveforms (a) in simulation (b) in experiment (250V/div& 2A/div)

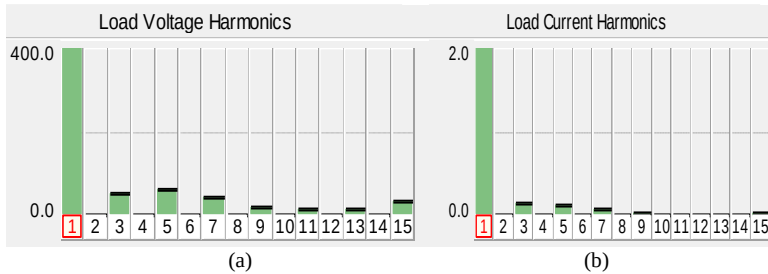


Fig. 13. Harmonic orders (a) output voltage (b) output current in simulation

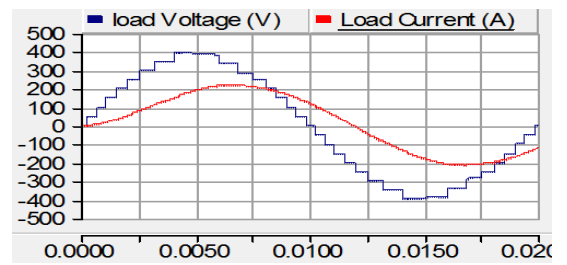


Fig. 12. Transient states of output waveforms in simulation

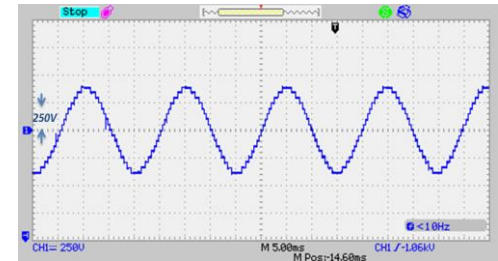


Fig. 14. Observed output voltage waveform at no-load condition (250V/div)

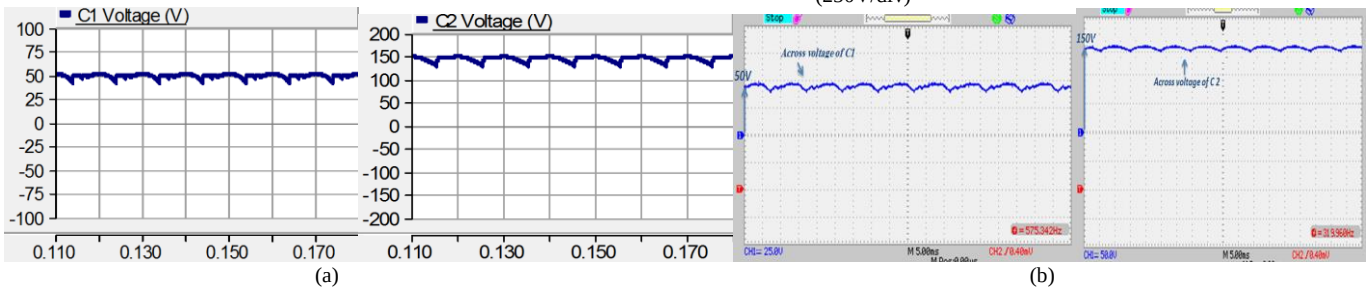


Fig. 15. Capacitors' voltage ripple waveforms for first case study (a) in simulation (b) in experiment (25 V/dev&50V/div)

As Figures show, the maximum amplitude of blocked voltage is 400V which can be tolerated by switches.

Table VII indicates the advantages of proposed topology in comparison with the first presented structure of [28] and [27] in terms of theoretical and measured value of output power and also overall efficiency based on (50). In this Table, the pertinent calculation of proposed topology have been done based on two different types of used power MOSFETs with two different values of R_{on} . Here, both of power switches can bear at least 400V blocked voltage with different value of nominal currents.

TABLE VII
THEORITICAL AND MEASURED VALUES OF OUTPUT POWER AND EFFICIENCY FOR PROPOSED TOPOLOGY AND [27-28]

Refs	Parameters				Type of used switches
	P_{out}		η		
	Theo	EXP	Theo	EXP	
Proposed topology	364[w]	352[w]	$\approx 91.5\%$	$\approx 88\%$	SPW47N60C3
	360[w]	348[w]	$\approx 90\%$	$\approx 87\%$	IRFP460
First structure of [28]	136[w]	129[w]	$\approx 90\%$	$\approx 86\%$	BUP306D
[27]	50[w]	$\approx 50[w]$	$\approx 83\%$	$\approx 83\%$	IRF540

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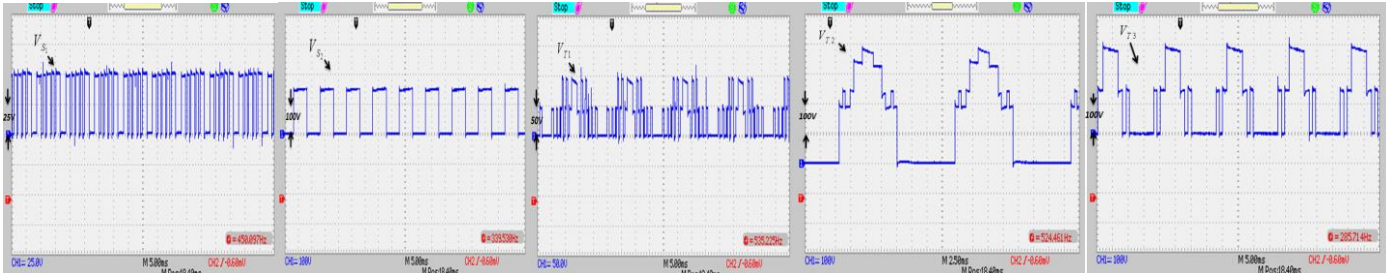


Fig. 16. Blocked voltage waveforms across switches of S_1 (25V/div), S_2 (100V/div), T_1 (50V/div), T_2 and T_3 (100V/div) from left to right in the experiment

B. Second case study

In order to corroborate the capability of proposed topology under the step load condition, an inductive load with value of $L = 320\text{mH}$ is connected to the output and the respective observed voltage and current waveforms are shown by Fig 17 (a). Therefore the maximum value of load current in this case, is about 4 A and also the amount of input power is 800W. In addition the dynamic behavior of step load for the output voltage and current waveforms from the resistive-inductive condition (first case study) to an inductive load condition (second case study) in simulation is demonstrated by Fig. 17 (b). Fig. 18 (a) and (b) show the simulation and experimental results for capacitors' current under inductive load condition, respectively. Here, the peak value of currents for both capacitors is about 4A without any considerable sudden spikes. Also, the respective variation of overall efficiency versus input power (p_{in}) for a resistive-inductive and severely inductive loads based on simulation and experimental results is curved in Fig. 19 (a) and (b), respectively. Here, the calculated and measured amount of output power under severely inductive load has better condition in contrast to resistive-inductive load because of negligible amount of current spike which is evident from Fig. 18 (a) and (b).

C. Third case study

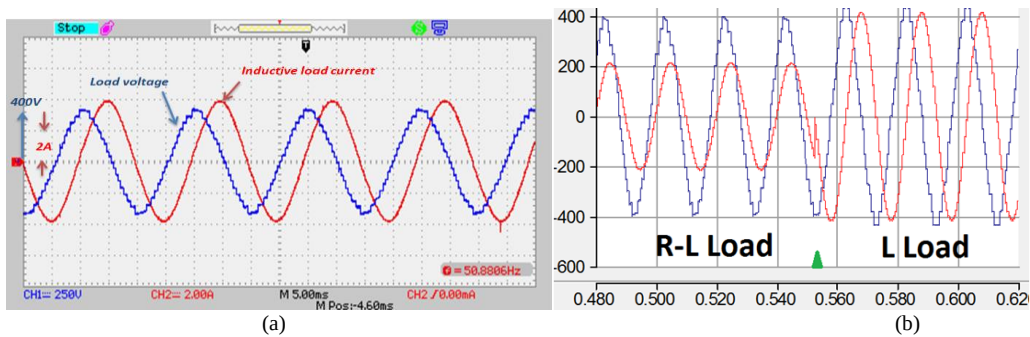


Fig. 17. Output voltage and current waveforms for (a) inductive load in experiment (250 V/div & 2 A/div) (b) sudden step load in simulation

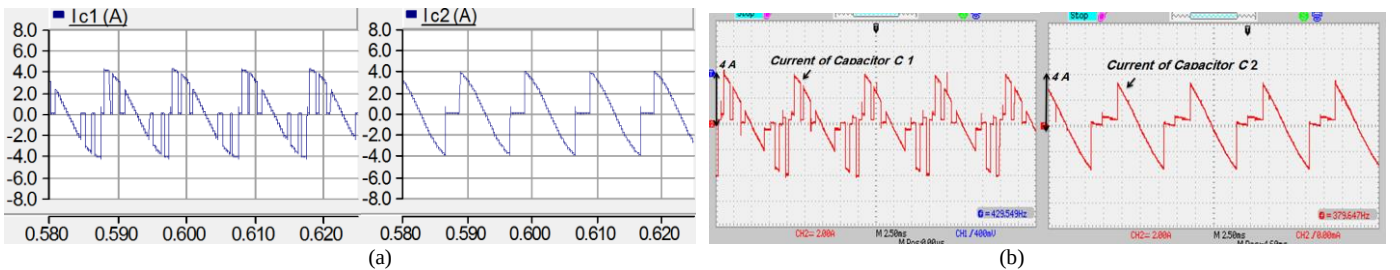


Fig. 18. Observed capacitors' current (a) in simulation (b) in experiment (2A/div)

In this case, to confirm the general performance of proposed SCC incorporated into proposed SMLI unit (Fig. 3), two same SCCs including two capacitors in each of them are considered. Therefore, based on (16) and with respect to $n = 2$, proposed SMLI can generate 49-level of output voltage by using four same capacitors. With hindsight (9), likewise two different dc voltage sources with values of 20V and 100V are needed. Fig. 20 (a) and (b) illustrate the built prototype and experimental results of output voltage and current waveforms, respectively. The load has been assumed same according to second case study. As can be seen, the maximum amplitude of load voltage and current are 480V and 3A, respectively. It is also obvious that, 49-level output voltage is quite similar to sinusoidal waveform with an appropriate THD.

Also, Fig 21 (a)-(d) show the across voltage waveform of each involved capacitor in upper and lower stages based on experimental observations, respectively which are fixed at the expected value of voltage by using proposed binary asymmetrical algorithm. As can be vividly seen, the across voltage of two capacitors in lower stage are balanced at 20V and 40V, while these values are 100V and 200V for capacitors in upper stage. Here, whole of the 49-level of output voltage is made with contribution of just two dc voltage sources which can prove the robust performance of proposed SCC in higher number of output voltage levels.

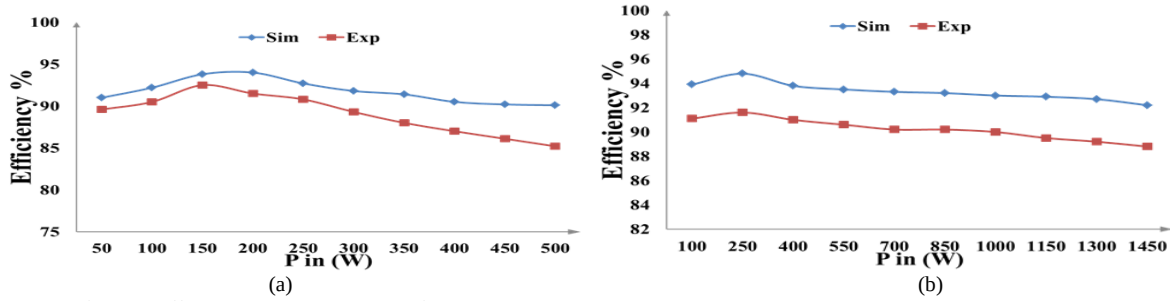


Fig. 19. Variation of overall efficiency versus input power for (a) resistive-inductive load (b) severely inductive load

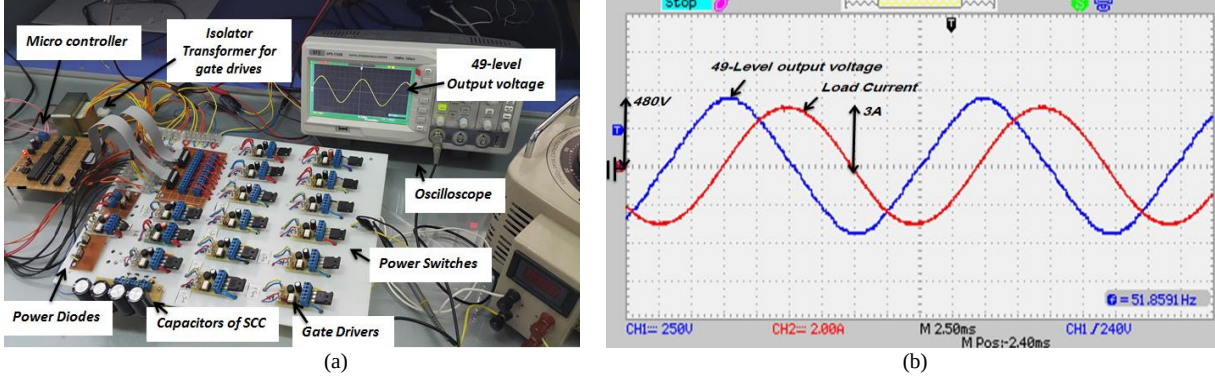


Fig. 20. (a) laboratory prototype (b) Output 49-level voltage and current waveforms in the experiment (250V/div & 2A/div)

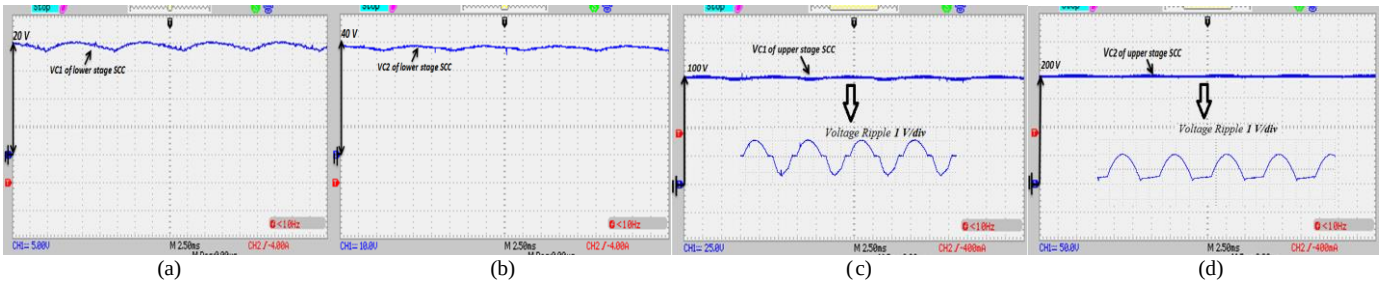


Fig. 21. Across voltage waveforms of capacitors in upper and lower stages of SCCs in proposed 49-level inverter (a) V_{C1} lower stage (5V/div) (b) V_{C2} lower stage (10V/div) (c) V_{C1} upper stage (25V/div) (d) V_{C2} upper stage (50V/div)

VIII. CONCLUSION

In this paper, at the first, a new reduced components SCC topology was presented which has boost capability remarkably and also can pass the reverse current for inductive loads through existing power switches. The voltage of all capacitors in this structure is balanced by binary asymmetrical algorithm. Next, a new sub-multilevel structure based on suggested SCC was proposed which can generate all of the voltage levels at the output (even and odd). In this case, the conventional output H-bridge cell used to convert the polarity of SCC units, has been removed, therefore number of required IGBTs and other involved components, are decreased. After that, an optimizing operation was presented which could obvious the number of required capacitors in each of SCC units that participate in the cascade sub-multilevel inverter (CSMLI) to generate maximum number of output voltage levels with less number of elements. Moreover comprehensive comparisons were given which prove the differences between improved symmetric and asymmetric CSMLIs in contrast to some of recently presented topologies in variety aspects. Finally, to confirm the performance and effectiveness of proposed CSMLI, several simulation and experimental results have been presented.

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Elyas Zamiri received his B.Sc. degree in Electrical Engineering from University of Guilan, Rasht, Iran in 2012 and his M.Sc. degree from University of Tabriz, Tabriz, Iran in 2014. His major researches include investigation on new topologies of multilevel voltage source inverters, switched-capacitor dc-dc converters and renewable energy systems.



Naser Vosoughi received his B.Sc. degree from Islamic Azad University, south Tehran branch, Tehran, Iran in 2011 and his M.Sc. degree from University of Tabriz, Tabriz, Iran in Electrical Engineering in 2014, where he is currently working toward his Ph.D. degree in Electrical and Computer Engineering department. His current researches include multilevel inverter, grid tie inverter, dc-dc switched capacitor and switched inductor converter, switching power supply, induction motor drive and MPC controller.



Seyed Hossein Hosseini (M'93) received Ph.D. degree in Elec. Eng. from INPL, France, in 1981. In 1981 he joined the Univ. of Tabriz, Iran, since 1995 he has been Professor in the Dept. of Elec. Eng. Univ. of Tabriz. From Sept. 1990 to Sept. 1991 he was Visiting Professor in the Univ. of Queensland Australia; from Sept. 1996 to Sept. 1997 he was Visiting Professor in the Univ. of Western Ontario Canada. His research interests include Power Electronic Converters, Applications of Power Electronics in Renewable Energy Systems, Reactive Power Control, Harmonics and Power Quality Compensation Systems such as SVC, UPQC, FACTS devices.



Reza Barzegarkhoo received his B.Sc. degree in Electrical Power Engineering from University of Guilan, Rasht, Iran in 2010 and his M.Sc. degree from Sahand University of Technology (SUT), Tabriz, Iran, in 2012. His major interests include design and control of power electronic converters, multilevel voltage source inverters, charge balancing control, switched-capacitor converters and photovoltaic systems.



Mehran Sabahi was born in Tabriz, Iran, in 1968. He received the B.S. degree in electronic engineering from the University of Tabriz, the M.S. degree in electrical engineering from Tehran University, Tehran, Iran, and the Ph.D. degree in electrical engineering from the University of Tabriz, in 1991, 1994, and 2009, respectively. In 2009, he joined the Faculty of Electrical and Computer Engineering, University of Tabriz, where he was an Assistant Professor from 2009 to 2013 and where he has been an Associate Professor since 2014. His current research interests include power electronic converters and renewable energy systems.